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10EC63

Sixth Semester B.E. Degree Examination, Dec.2015/Jan.2016
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting THREE from PART-A and TWO from PART-B.***

PART – A

1 a. Explain channel length modulation effect and derive an expression for finite output resistance of a MOSFET in saturation region. **(08 Marks)**

b. Analyze the circuit shown in Fig. 1(b) to determine the voltages at all nodes and the currents through all branches let the nMOSFET $V_t = 1V$ and $k_n' \frac{W}{L} = 1mA/V^2$. Assume $\lambda = 0$. **(08 Marks)**

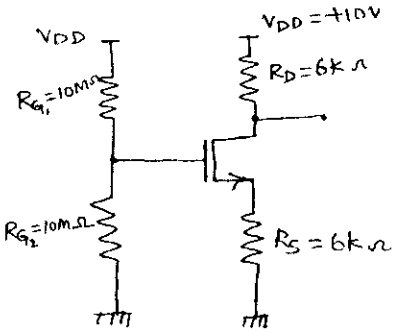

Fig.Q1(b)

c. Explain briefly biasing using constant current source. **(04 Marks)**

2 a. Derive analytical expressions for transfer characteristics of CS amplifier. **(08 Marks)**

b. Fig. Q2(b) shows a discrete CS MOSFET amplifier utilizing the drain to gate feedback biasing arrangement. Determine the small signal voltage. Gain its input resistance and the largest allowable input signal. Let $V_t = 1.5V$, $k_n' \frac{W}{L} = 0.25mA/V^2$ and $V_A = 50V$.

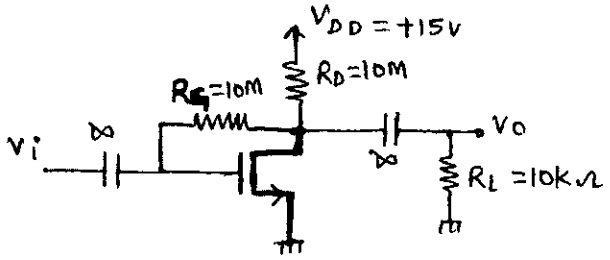

Fig.Q2(b) **(07 Marks)**

c. Briefly explain common drain amplifier. **(05 Marks)**

3 a. With neat circuit diagram, explain basic BJT current mirror and derive an expression for CT ratio of BJT current mirror for finite β. **(08 Marks)**

b. Derive an expression for 3dB frequency f_H for an amplifier having 2 poles and 2 zeros. **(08 Marks)**

c. Explain millers theorem. **(04 Marks)**

4 a. Briefly explain common source amplifier with active load. **(10 Marks)**

b. With neat circuit diagram, explain the MOS cascode amplifier. **(10 Marks)**

PART – B

5 a. Explain the operation of MOS differential pair with a common mode input voltage. **(07 Marks)**

b. Briefly explain the basic operation of BJT differential pair with neat circuit diagram. **(07 Marks)**

c. Explain two stage CMOS OPAMP. **(06 Marks)**

6 a. Write a note on gain desensitivity and bandwidth extension. **(06 Marks)**

b. Draw the ideal structure and equivalent circuit of the series shunt feedback amplifier and explain. **(10 Marks)**

c. Write a note on amplifier with a single pole response. **(04 Marks)**

7 A Derive an expression for the closed load gain (v_0/v_i) of the circuit shown in Fig. Q7(a). Assume the OPAMP is ideal. **(06 Marks)**

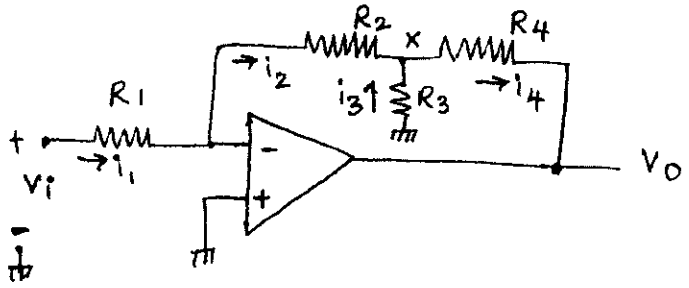

Fig.Q7(a)

b. Explain instrumentation amplifier with neat circuit diagram. **(08 Marks)**

c. With neat circuit diagram, explain antilog amplifier. **(06 Marks)**

8 a. A CMOS inverter fabricated in a 0.25 μm process has C_{ox} = 6 f F/μm^2, $\mu_n C_{ox}$ = 115 μA/v^2, $\mu_p C_{ox}$ = 30 μA, $v_{tn} = -v_{tp}$ = 0.4v and V_{DD} = 2.5v. The W/L ratio of Q_n is 0.375 μm/0.25μm, and that for Q_p is 1.125μm/0.25 μm. The gate – source and gate drain overlap capacitances are specified to be 0.3 f F/μm of gate width. Further the effective value of drain body capacitances are C_{dbn} = 1fF and C_{dbp} = 1 fF. The wiring capacitance C_W = 0.2f F. Find t_{PHL}, t_{PLH} and t_p. **(10 Marks)**

b. Implement $F = \overline{AB + \overline{AB}}$ using AOI. **(05 Marks)**

c. Explain two single input domino CMOS gate. **(05 Marks)**

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